# **TSO-CC** Specification

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# **1** Introduction

This document provides a detailed specification of the TSO-CC protocol [EN14].

# 2 Storage Requirements

Table 1 is a summary of storage requirements and introduces parameter names and literals used in the protocol description.

# 3 Assumptions & Definitions

1. The protocol requires distinguishing valid and invalid timestamps (b.ts). In the following specification  $\emptyset$  is used to denote an invalid entry. In our implementation, we use 0 to denote an invalid timestamp, which means the smallest valid timestamp is 1.

	Per node	Per line <b>b</b>
L1		
	1. current timestamp, $B_{ts}$ bits	1. number of accesses $b.acnt$ , $B_{maxacc}$ bits
	2. write-group counter, $B_{write-group}$ bits	2. last-written timestamp <b>b.ts</b> , $B_{ts}$ bits
	3. current epoch-id, $B_{epoch-id}$ bits	
	4. timestamp-table ts_L1[n], $n \leq C_{L1}$ entries	
	5. epoch-ids epoch_ids_L1[n], $n = C_{L1}$ entries	
	6. timestamp-table ts_L2[n], $n \leq C_{L2-tiles}$ entries (for SharedRO)	
	7. epoch-ids epoch_ids_L2[n], $n = C_{L2-tiles}$ entries (for SharedRO)	
L2		
	1. last-seen timestamp-table ts_L1[n], $n = C_{L1}$ entries	1. timestamp b.ts, $B_{ts}$ bits 2. owner (Exclusive) last-writer (Shared)
	2. epoch-ids epoch_ids_L1[n], $n = C_{L1}$ entries	coarse vector (SharedRO) as b.owner, $\lceil log(C_{L1}) \rceil$ bits
	3. current timestamp, $B_{ts}$ bits (for SharedRO)	
	4. current epoch-id, $B_{epoch-id}$ bits (for SharedRO)	
	5. increment-timestamp-flags, 2 bits (for SharedRO)	

Table 1: Coherence specific storage requirements

- 2.  $\mathsf{DataS}, \mathsf{DataX}$  and  $\mathsf{Data}$  messages are expected to carry data.
- 3. A receive message action is of the format: source?Message.
- 4. A send message action is of the format: destination!Message.
- 5. A batch transition of all lines in states State1, State2, ... to state NextState is abbreviated tr\_all {State1, State2, ...} NextState.

# 4 Protocol State Table

The state transition tables can be found in Tables 2 and 3. The following sections provide notes about events in the Tables marked by the respective raised number.

#### 4.1 Private Cache Controller

- 1. We can't just set the state to Invalid, as the directory might have gotten a read and forwarded the request to us. So we must write back, and wait for Ack to ensure that the line propagated to the L2, and thus no more Fwd requests are outstanding.
- 2. If  $B_{write-group} = 0$ , in the presence of non-infinite timestamps, the comparison operator cannot be <, as it would violate correctness. This is due to how timestamp resets are dealt with in the L2 (see §5.3).
- 3. Must reset timestamp, in case the line has since been evicted from L2 and we obtain it in Exclusive. If this is the case, the line may have been modified by another node; now, if we get a FwdX request, the old timestamp must not be forwarded.

#### 4.2 Directory Controller

- 1. Reuse the block's b.owner bits to maintain a superset of SharedRO sharers: each bit is a pointer to  $\left\lceil \frac{C_{L1}}{\lceil log(C_{L1}) \rceil} \right\rceil$  sharers.
- 2. Checking if a line's timestamp in the L2 is **decayed**. In order to allow **Shared** blocks which have not been written to in a long time to transition to **SharedRO**, we can use the timestamp *b.ts* and compare against the owner's entry in the last-seen table: check if a fixed period has passed between the last-seen timestamp and when the line was updated according to *b.ts*.

 $\mathsf{ts\_L1}[\mathsf{b.owner}] > 2^{B_{ts}-n} \land \mathsf{b.ts} \le \mathsf{ts\_L1}[\mathsf{b.owner}] - 2^{B_{ts}-n}$ 

#### Table 2: TSO Coherence private (L1) cache controller – table of states and events.

HeadWriteEviceare (Data) (state, or constant) (st			1	14046 2: 100 00	herence private (Er) cach		le of states and events.			
		Read	Write	Evict	src?DataS(state, └→ owner, ts)	src?DataX(owner	, src?FwdS(dst)	src?FwdX(dst)	src?Ack	src?InvRO
$ \begin{array}{c c c c c c } & $$ $$ $$ $$ $$ $$ $$ $$ $$ $$ $$ $$ $$	Invalid	dir!GetS:	dir!GetX:			. ,				dir!AckRO:
$\begin{array}{ c c c c } \hline \hline \mbox{Waits} & \mbox{Mit} & \mbox{Mit}$		b ts $\leftarrow \emptyset$	update bits							
Exclusive       hit:       bit:       bit:       diffects:       diffects: <thdiffect:< th="">       diffects:       diffec</thdiffect:<>		$\rightarrow$ WaitS	$\rightarrow$ WaitX							
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Exclusivo	hit:	hit:	dirl DutE:			det/DataS(SharodPO	det/DataX(colf		dirlAckBO
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c } \hline \hline \begin{tabular}{ c c c c c } \hline \hline \begin$	LACIUSIVE	inc,	inc,							ull:Ackito,
$ \begin{array}{ c c c c } \hline  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c  &  c c c c$			update b.ts;	$\rightarrow$ vvaltEI;			$\rightarrow$ self, D.ts);	$\rightarrow$ D.ts, 1);		
Modifiedhit: update bis; treament backt; bis: 			$\rightarrow$ iviodified;				dir!Ack(0);	$\rightarrow$ Shared;		
Modified       ht:							$\rightarrow$ SharedRO;			
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Modified	hit;	hit;	dir!Data(b.ts);			dst!DataS(Shared,	dst!DataX(self,		dir!AckRO;
$\begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$			update b.ts;	$\rightarrow$ WaitMI;			└→ self, b.ts);	└→ b.ts, 1);		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $							dir!Data(b.ts);	$\rightarrow$ Shared;		
Shared       if b.art       maxic then increment b.art; ht; wints $\rightarrow$ Invalid; wints; $\rightarrow$ Waits; $\rightarrow$							$\rightarrow$ Shared:			
Short of the increment bacht: ht: the increment bacht bacht: ht increment bacht bacht bacht bacht: ht increment bacht	Shared	if b acnt < maxac then	dir!GetX.	→ Invalid <sup>.</sup>						dir!AckRO <sup>.</sup>
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Sharea	increment b acnt:	undate b ts:	/ invalia,						un nicht tert ter,
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		hit:	$\sqrt{M/2i+Y}$							
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		, iii.,	$\rightarrow$ vvalu $\wedge$ ,							
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		else								
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		dir!GetS;								
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		b.ts $\leftarrow \emptyset$ ; <sup>3</sup>								
endiforder <th< td=""><td></td><td><math>\rightarrow</math> WaitS;</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></th<>		$\rightarrow$ WaitS;								
SharedRO       hit:       update b.ts; dirlAckRO; $\rightarrow$ Invalid;         WaitS       stall;       stall;       stall;       stall;       copy_data; hit; reset b.acnt; dirlAckRO; $\rightarrow$ WaitSROI       stall;       stall;       stall;       dirlAckRO; $\rightarrow$ WaitSROI       dirlAckRO; $\rightarrow$ WaitSROI         WaitSROI       stall;       stall;       stall;       stall;       copy_data; hit; reset b.acnt; dirlAckRO; $\rightarrow$ Invalid;       reset b.acnt; dirlAckRO;       dirlAckRO; $\rightarrow$ WaitSROI       dirlAckRO; $\rightarrow$ WaitSROI         WaitSROI       stall;       stall;       stall;       copy_data; hit; reset b.acnt; dirlAckRO; $\rightarrow$ Invalid; $\rightarrow$ Invalid;       stall;       dirlAckRO; $\rightarrow$ Modified;         WaitX       stall;       stall;       stall;       copy_data; hit; reset b.acnt; dirlAckRO; $\rightarrow$ Invalid; $\rightarrow$ Invalid;       dirlAckRO; $\rightarrow$ Invalid; $\rightarrow$ Invalid;       dirlAckRO; $\rightarrow$ Invalid;       dirlAckRO;		endif								
$\begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	SharedRO	hit;	update b.ts;	$\rightarrow$ Invalid;						dir!AckRO;
$\begin{array}{ c c c c c c } \hline \hline$			dir!GetX:							$\rightarrow$ Invalid:
WaitSstall;stall;copdata; hit; reset bacnt; if state = Exclusive then dirlAck(0); endif $\rightarrow$ state;stall;copdata; hit; reset bacnt; if state = Exclusive then dirlAck(0); elf state = Exclusive then dirlAck(0); elf state = ShareRO then $\rightarrow$ state;dirlAckRO;WaitSstall;stall;stall;copdata; hit; reset bacn; if state = Exclusive then dirlAck(0); elf state = ShareRO then $\rightarrow$ state;copydata; hit; reset bacn; if state = ShareRO then $\rightarrow$ state;copydata; hit; reset bacn; elf state = ShareRO then $\rightarrow$ state;dirlAckRO;dirlAckRO;WaitXstall;stall;stall;stall;copydata; hit; reset bacn; $\rightarrow$ state;copydata; hit; reset bacn; $\rightarrow$ state;dirlAckRO;WaitXstall;stall;stall;stall;copydata; hit; reset bacn; $\rightarrow$ state;dirlAckRO;WaitEIstall;stall;stall;copydata; hit; reset bacn; $\rightarrow$ state;dirlAckRO;WaitMIstall;stall;stall;copydata; hit; reset bacn; $\rightarrow$ state;dirlAckRO;WaitMIstall;stall;stall;dirlAckRO;WaitMIstall;stall;for one = $0 \land ts \neq 0$ then is_L2[ser] < ts then is_L2[ser] < ts then rs_all (Shared) Invalid;dirlAckRO; $\rightarrow$ Invalid;dirlAckRO;UDataSIf one = $0 \land ts \neq 0$ then is_L2[ser] < ts then rs_all (Shared) Invalid;eif one fits ts all;eif one fits ts all;eif one fits ts all;UDataSIf one one is the stall;If one fi			$\rightarrow$ Wait X							,,
$ \begin{aligned} \begin{array}{c} \text{WaitSROI} \\ Wait$	WaitS	stall	stall	stall	conv. data: hit:					dirlAckRO.
$ \begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Waito	Stan,	Stan,	Stall,	rosot b acet:					WaitSPOL
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$					feset D.acht,					$\rightarrow$ waits (0),
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$					If state = Exclusive then $\frac{1}{2}$					
WaitSROIstall;stall;stall;copy_data; hit; reset b.acn; if stale = SharedRO then $\rightarrow$ invalid; endifdirlAckRO;WaitXstall;stall;stall;copy_data; hit; reset b.acn; if stale = SharedRO then $\rightarrow$ invalid; endif $\rightarrow$ state;copy_data; hit; reset b.acn; eilf state = SharedRO then $\rightarrow$ invalid; endif $\rightarrow$ state;copy_data; hit; reset b.acn; eilf state = SharedRO then $\rightarrow$ invalid; endif $\rightarrow$ state;copy_data; hit; reset b.acn; eilf reset b.acn; <br< td=""><td></td><td></td><td></td><td></td><td>dir!Ack(0);</td><td></td><td></td><td></td><td></td><td></td></br<>					dir!Ack(0);					
WaitSROIstall;stall; $\rightarrow$ state; $\rightarrow$ st					endif					
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $					ightarrow state;					
$ \begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	WaitSROI	stall;	stall;	stall;	copy_data; hit;					dir!AckRO;
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$					reset b.acnt;					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$					if state = Exclusive then					
$ \begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$					dir!Ack(0):					
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c } \hline \end{tabular} & \end{tabular} &$					elif state - SharedRO then					
$\begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$					$\rightarrow$ Invalid:					
$\begin{array}{ c c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$					andif					
WaitXstall;stall;stall;stall;copy_data; hit; reset b.acnt; dir!Ack[ackC); $\rightarrow$ Modified;dir!AckRO;WaitZIstall;stall;stall;stall;dir!AckRO;WaitEIstall;stall;stall;stall;dir!AckRO;WaitEIstall;stall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;WaitMIstall;stall;stall;stall;DataSif owner = $\emptyset \land ts \neq \emptyset$ then ts_L2[src] < ts then ts_L2[src] < ts; tr_all {Shared} Invalid;dir!AckRO;WaitXWaitXlif owner = $\emptyset \land ts \neq \emptyset$ then ts_L2[src] < ts; tr_all {Shared} Invalid;dir!AckRO;WaitXmainlif owner = $\emptyset \land ts \neq \emptyset$ then ts_L2[src] < ts; endifdir!AckRO;WaitXmainlif ownerdir!AckRO;WaitXmain </td <td></td> <td></td> <td></td> <td></td> <td>enun</td> <td></td> <td></td> <td></td> <td></td> <td></td>					enun					
WaitXStall;Stall;Stall;Stall; $Cop_dat; nt; rest b.acnt; dir!Ack(ackc); \rightarrow Modified;dir!Ack(x, ckc); \rightarrow Modified;dir!Ack(x, ckc); \rightarrow Modified;WaitElstall;stall;stall;stall;dir!Ack(ackc); \rightarrow Modified;dir!Ack(ackc); \rightarrow Modified;dir!Ack(x, ckc); \rightarrow Modified;WaitMIstall;stall;stall;stall;dir!AckRO;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;dir!AckRO;WaitMIstall;stall;stall;dir!AckRO;DataSfif owner = \emptyset \land ts \neq \emptyset thents_L2[src] < ts thents_L2[src] < ts; tr_all {Shared} Invalid;$					$\rightarrow$ state;	1			_	
$ \begin{array}{ c c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	WaltA	stall;	stall;	stall;		copy_data; nit;				dir!AckRO;
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c c c } \hline \end{tabular} \\ \hline \end{tabular} \\$						reset b.acnt;				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$						dir!Ack(ackc);				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $						$\rightarrow$ Modified;				
$ \begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	WaitEl	stall;	stall;	stall;			dst!DataS(SharedRO,	dst!DataX(self,	$\rightarrow$ Invalid;	dir!AckRO;
$ \begin{array}{ c c c c c c c } \hline \end{tabular} \hline t$							└→ self, b.ts);	↓ b.ts, 0);		
WaitMIstall;stall;stall;stall;dir!AckRO; $WaitMI$ $stall;$ $stal$							$\rightarrow$ Invalid:	$\rightarrow$ Invalid:		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	WaitMI	stall	stall	stall			dst!DataS(Shared	dst!DataX(self	$\rightarrow$ Invalid <sup>.</sup>	dir!AckRO <sup>.</sup>
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			Stan,	Scan,			colf b ts):	b + c = 0	,,	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$										
$ \begin{array}{c} DataS \\ & @ WaitS, WaitSROI \\ & DataX \\ & & @ WaitX \end{array} \end{array}  \begin{array}{c} \text{if owner} = \varnothing \land ts \neq \varnothing \text{ then} \\ & \text{if } ts\_L2[src] < ts then \\ & ts\_L2[src] \leftarrow ts; \\ & tr\_all \{Shared\} Invalid; \\ & endif \\ & \ddots \end{array}  \begin{array}{c} \cdots \\ & elif owner \neq self \land (ts = \varnothing \lor ts\_L1[owner] \leq ts) then^2 \\ & \text{if } ts \neq \varnothing then \\ & ts\_L1[owner] \leftarrow ts; \\ & endif \\ & \cdots \end{array}  \begin{array}{c} endif \\ & tr\_all \{Shared\} Invalid; \\ & endif \\ & endif \end{array} $	L						$\rightarrow$ invalid;			
$ \begin{array}{ c c c c c } & @ WaitS, WaitSROI & & if ts\_L2[src] < ts then & & ts\_L2[src] < ts then & & ts\_L2[src] < ts; & & & ts\_L2[src] < ts; & & & ts\_L2[src] < ts; & & & ts\_L1[owner] \le ts) then^2 & & & if ts \neq \emptyset then & & & ts\_L1[owner] < ts) then^2 & & & & ts\_L1[owner] < ts & & & ts\_L1[owner] < ts & & & ts\_L1[owner] < ts & & & & & & ts\_L1[owner] < ts & & & & & & & & & ts \\ & & & & & & & & & & & & & & & & & & $		DataS		if owner $= \emptyset \land ts \neq$	Ø then					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		👃 🛛 @ WaitS, WaitSRO	)I I	if $ts_L2[src] < ts$	then	elif	$owner \neq self \land (ts = \varnothing \lor ts_{})$	$L1[owner] \le ts)$ then	1 <sup>2</sup>	
<pre>     @ WaitX     tr_all {Shared} Invalid;     endif     tr_all {Shared} Invalid;     endif     tr_all {Shared} Invalid;     endif     tr_all {Shared} Invalid;     endif </pre>		DataX		$ts\_L2[src] \leftarrow ts$	,	if	ts $\neq \emptyset$ then	- *		
endif endif tr_all {Shared} Invalid; endif		6 WaitX		tr all {Shared} Ir	ivalid;		ts L1[owner] $\leftarrow$ ts:			
tr_all {Shared} Invalid;				endif		er	ndif			
endif						tr	all {Shared} Invalid			
						endi	<u> </u>			

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#### Table 3: Directory (L2) controller – table of states and events.

		Table 9. Birecto		of states and events.		
	p?GetS	p?GetX	p?Data(ts)	p?Ack(c)	p?PutE	p?AckRO
Invalid	p!DataS(Exclusive, ∅, ∅);	p!DataX(Ø, Ø, 0);				
	b.owner $\leftarrow$ p;	b.owner $\leftarrow$ p;				
	$b.ts \leftarrow \emptyset;$	$b.ts \leftarrow \emptyset;$				
	$\rightarrow$ WaitE1;	$\rightarrow$ WaitE1;				
Uncached	p!DataS(Exclusive, b.owner, b.ts);	p!DataX(b.owner, b.ts, 0);				
	b.owner $\leftarrow$ p;	b.owner $\leftarrow$ p;				
	$b.ts \leftarrow \emptyset;$	b.ts $\leftarrow \emptyset$ ;				
	$\rightarrow$ WaitE1;	$\rightarrow$ WaitE1;				
Exclusive	b.owner!FwdS(p):	b.owner!FwdX(p):	copy data:		p!Ack:	
	tbe sharers $\leftarrow \{p\}$ :	b.owner $\leftarrow p$ :	p!Ack:		$\rightarrow$ Uncached:	
	$\rightarrow$ WaitS	h ts $\leftarrow \emptyset$	$h ts \leftarrow ts$		, encuence,	
	, wates,	$\rightarrow$ W/aitE2:	$\rightarrow$ Uncached:			
Shared	if expired b to $\frac{1}{2}$ decayed b to the then $\frac{2}{2}$	p DataX(b, owner, b, ts, 0);	/ Oncached,			
Shared	h expired bits v decayed bits then	p:Data(b.owner, b.ts, 0),				
	b.owner $\leftarrow \{p\};$	b.owner $\leftarrow$ p;				
	update D.ts; $u \mid D_{abs} S(S_{base} \mid D_{abs} \mid A_{bbs})$	$D.ls \leftarrow \emptyset;$				
	$p!DataS(SharedRO, \emptyset, b.ts);$	$\rightarrow$ vvaitE1;				
	$\rightarrow$ Shared RO;					
	else					
	p!DataS(Shared, b.owner, b.ts);					
	endif					
SharedRO	$p!DataS(SharedRO, \emptyset, b.ts);$	dst $\leftarrow \{q \mid q \in b.owner \land q \neq p\};$				
	b.owner $\leftarrow$ b.owner $\cup \{p\};^{\perp}$	dst!InvRO;				
		$tbe.need\_acks \leftarrow  dst ;$				
		b.owner $\leftarrow$ p; $\rightarrow$ WaitEn;				
WaitE1	stall;	stall;	if $p \neq b$ .owner then	$\rightarrow$ Exclusive;	if $p \neq b$ .owner then	
			$\rightarrow$ Exclusive;		$\rightarrow$ Exclusive;	
			else		else	
			copy_data;		p!Ack;	
			p!Ack;		$\rightarrow$ WaitU1;	
			b.ts $\leftarrow$ ts;		endif	
			$\rightarrow$ WaitU1:			
			endif			
WaitF2	stall <sup>.</sup>	stall <sup>.</sup>	if $p \neq b$ owner then	if $c = 1$ then	if $p \neq b$ owner then	
	otan,	ordin,	$\rightarrow$ Wait F1	$\rightarrow$ Exclusive	$\rightarrow$ Wait E1:	
			else	else	else	
			conv data:	WoitE1	plAck:	
			plAck		) M/ai+U2	
			p:ACK,	enun	$\rightarrow$ WaltO2,	
			$D.ls \leftarrow ls;$		enan	
			$\rightarrow$ VValtU2;			
			endif			
WaitU1	stall;	stall;	$\rightarrow$ Uncached;	$\rightarrow$ Uncached;	$\rightarrow$ Uncached;	
WaitU2	stall;	stall;	$\rightarrow$ WaitU1;	if $c = 1$ then	$\rightarrow$ WaitU1;	
				$\rightarrow$ Uncached;		
				else		
				$\rightarrow$ WaitU1;		
				endif		
WaitEn	stall;	stall;				tbe.need_acks;
						if tbe.need_acks = 0 then
						b.owner! $\overline{D}$ ataX( $\emptyset$ , b.ts, 0);
						b.ts $\leftarrow \emptyset$ ;
						$\rightarrow$ WaitE1;
						endif
WaitS	stall <sup>.</sup>	stall	copy data:	b owner $\leftarrow$ the sharers $   \{p\}$	b owner $\leftarrow$ the sharers:	
			h ts $\leftarrow$ ts	undate b ts:	undate b ts:	
			$\rightarrow$ Shared:	$\rightarrow$ Shared BO	$\rightarrow$ Shared RO	
			/ Shareu,	/ Sharcurto,		

### 5 Additional Rules & Optimizations

The following is a list of additional rules and optimizations, which have an impact on both L1 and L2 controllers; this completes the full protocol description.

#### 5.1 Cache inclusivity & evictions

Evictions from the L2 are omitted from the transition table; the following must hold: upon eviction of lines from the L2, inclusivity must be maintained for lines which are tracked by the L2 (Exclusive and SharedRO).

#### 5.2 Timestamp table size relaxations

The L1's timestamp-tables ts\_L1 and ts\_L2 do not need to be able to hold as many entries as there are respective nodes. Applying an eviction policy to evict entries from the timestamp-tables allows to have a reduced-size timestamp-table.

#### 5.3 Effect of L1 timestamp update

To **update** a timestamp in the L1 means assigning the locally maintained timestamp to the line, and also increment this timestamp based on either of the following policies:

- 1. Always (write-group = 1).
- 2. Write-groups: If constant number of writes falling under the same timestamp reached.

Timestamp overflows in the L1 are dealt with sending out a TimestampReset broadcast to L1s and L2 tiles:

- 1. Each L1 invalidates ts\_L1[src] on receiving a TimestampReset.
- 2. Every L2 tile must also maintain a table ts\_L1 of last-seen timestamps; ts\_L1[src] is updated on every b.ts ← ts, if ts is newer than the existing last-seen timestamp entry from an L1; on receiving a TimestampReset the respective entry is invalidated. The table of last-seen timestamps must be able to hold, unlike the L1's timestamp-tables, the full list of timestamps of every possible L1.
- 3. The L2 will assign a response message b.ts if the *last-seen timestamp from the owner is larger* or equal to the line's timestamp (not **expired**), the smallest valid timestamp ( $\emptyset$  is valid, but degrades performance) otherwise. Similarly for **all** L1 data messages by comparing against L1's own timestamp.

#### 5.4 Effect of L2 timestamp update

To update a timestamp in the L2 (for SharedRO) means assigning the L2-local timestamp to the line and incrementing the timestamp under the following conditions:

- from-Invalid, check against in WaitS to SharedRO transition: after a L2 eviction of a dirty line; after a GetS event in Uncached where b.ts ≠ Ø before resetting b.ts.
- from-Shared, check against in Shared to SharedRO transition: after a block transitions to Shared.

Maintain a bit for each from-condition to signify if the timestamp should be incremented on the next update or not, resetting *all* bits after the increment was performed.

In essence, the L2's timestamp should always be increment after a transition which can lead to a block ending up in the SharedRO state, but need not actually be incremented until the first block transitions to SharedRO.

It is possible to use only one bit for all conditions, but this would cause unnecessary timestamp increments when a cache line transitions to SharedRO based on the not-modified rule, as transitions to Shared are quite common, but Shared to SharedRO may not be, therefore it makes sense to maintain extra bits for each observed transition that may lead back to a SharedRO state, but only check the condition at the appropriate nearest transition to SharedRO.

To abstract the condition when to increment a L2-timestamp further (define  $\rightarrow$  as the happensbefore relation): if a set of writes  $\mathbb{W} \rightarrow$  set of transitions  $\mathbb{T}$  that can cause likely transitions  $\mathbb{R}$  to SharedRO, but we can not keep track of which blocks are affected, the system should remember that  $\mathbb{T}$  happened so that upon the first transition in  $\mathbb{R}$  we can allow L1s to deduce  $\mathbb{W} \rightarrow^+ \mathbb{R}$ . For two timestamps t and t', if t < t' then  $\mathbb{W} \rightarrow \mathbb{T} \rightarrow \mathbb{R} \rightarrow \mathbb{W}' \rightarrow \mathbb{T}' \rightarrow \mathbb{R}'$ ; in order to make visible all writes from  $\mathbb{W}'$  the L1 needs to self-invalidate on  $\mathbb{R}'$ , if the largest timestamp value from the L2 it has seen is only t.

Dealing with timestamp overflows:

- 1. Timestamp overflows in the L2 are dealt with sending out a TimestampReset broadcast and each L1 resetting ts\_L2[src]. To not send invalid timestamps, like in §5.3, the L2 will assign a response message b.ts if the *current L2-local timestamp is larger or equal to the line's timestamp*, the smallest valid timestamp ( $\emptyset$  is valid, but degrades performance) otherwise; in case the smallest valid timestamp is used, the next timestamp assigned to a line after an overflow must always be larger than the smallest valid timestamp.
- 2. In a NUCA architecture, it will be necessary to either propagate all increments to the L2-local timestamp across all tiles, or each L2 tile maintains its own timestamp, and the L1s maintain a ts\_L2 entry per tile or cluster of tiles in a separate table.

#### 5.5 TimestampReset races

To resolve TimestampReset races, without requiring the sender of a TimestampReset to wait for acks, if we can assume a bounded time on message propagation delay:

- 1. Every node in the system (L1s and L2 tiles) maintains an epoch\_id, which is set to a value different than the previous value on sending a TimestampReset; the TimestampReset message contains the new epoch\_id. The number of bits required per epoch\_id must be large enough to eliminate the probability of having more than one TimestampReset message with the same epoch\_id in-flight, but small enough to satisfy storage requirements.
- 2. The L1s maintain a table of epoch\_ids with entries for every L1 and L2 tiles in the system.
- 3. The L2 tiles each maintain a table of epoch\_ids with entries for every L1.
- 4. On receiving a TimestampReset message, the sender's entry in the respective timestamp-table is invalidated but the epoch\_ids entry for the sender is updated with the epoch\_id that was received along with the TimestampReset message.
- 5. An epoch\_id is sent with every Data, DataS and DataX message:
  - If the message originates from an L1, it is the L1s own epoch\_id.
  - If the message originates from the L2, and owner ≠ Ø, the entry in epoch\_ids\_L1[b.owner] is assigned.
  - If the message originates from the L2, and owner = Ø ∧ ts ≠ Ø, the L2's epoch\_id is assigned.

- 6. The L2 updates epoch\_ids\_L1[p] along with every b.ts ← ts. If epoch\_ids\_L1[p] ≠ epoch\_id, the last-seen entry in ts\_L1 must be updated (timestamp reset).
- 7. On receiving a DataS or DataX message, before the check for potential acquires, the L1 must perform the following check:

If a self-invalidation is possible due to seeing a newer value than in the timestamp-tables  $ts\_L1$  or  $ts\_L2$  respectively, but not having done this check yet, check if the currently held epoch-id for the line's source is valid or not, if not, invalidate the entry in the timestamp-table, essentially performing the same action if a TimestampReset is received.

#### 5.6 Out-of-Order Pipeline Interaction

The description thus far is compatible with a core with a FIFO write-buffer, but without load speculation (in-order). Introducing load speculation, e.g. via a load-queue (LQ), will require forwarding invalidations accordingly.

- 1. Similarly to other conventional eager protocols, any invalidation (self-invalidation, forced miss, or otherwise) must be forwarded to a LQ.
- 2. Upon self-invalidation, for all lines in WaitS state, an invalidation must also be forwarded to the LQ. To avoid a retry still hitting in a stale cache line, we propose either:
  - a) Adding an additional bit of information to a request from a LQ to denote a retry. In case of a Read+retry, the protocol forces a miss in the Shared state only. This option offers potentially higher performance, as the LQ has more information about which instructions are potentially violated or not, and could still hit (more than once) in a stale cache line if no violation is detected.
  - b) Sinking the self-invalidation and transitioning the line to Invalid if the response is Shared data. A retry will miss and fetch the correct data. This option is more conservative, as unnecessary invalidations take place; unlike LQ, the coherence protocol has no information about the order of in-flight instructions.

The above is required to deal with the following case (and its variants): consider the example in Figure 1. Assume the LQ issues the Read request for 2b first (transition to WaitS), the L2 cache responds with the initial data but the response message remains in transit. Next, 1a and 1b are performed (and committed), and then 2a is issued and receives the value produced by 1b. The acquire at 2a causes self-invalidation. However, the response for 2b arrives with stale data, causing a TSO violation. The above options prevent this case from manifesting.

init: $x = 0$ , $y = 0$				
Thread 1	Thread 2			
1a. x $\leftarrow$ 1	2a. r1 $\leftarrow$ y			
1b. y $\leftarrow$ 1	2b. r2 $\leftarrow$ x			

Figure 1: Message passing pattern.

# 6 Changelog

**Dec. 17, 2015:** Add section §5.6 on out-of-order pipeline interaction. We would like to thank the authors of CCICheck [Man+15], who informed us that interaction with OOO was not clear; they further suggested that a corner case with speculative loads (§5.6, case 2.) may exist if not dealt with. We verified this using McVerSi [EN16] in Gem5: using the regular network model used, the bug does not manifest as the maximum bound on messages in transit prevents this; however, the problem manifests (if not dealt with as described) when adding large randomized interconnect delays.

### References

- [EN14] M. Elver and V. Nagarajan. "TSO-CC: Consistency directed cache coherence for TSO". In: HPCA. (Orlando, FL, USA). Feb. 2014. URL: http://ac.marcoelver.com/res/research/ tsocc/hpca14\_tso-cc.pdf.
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- [Man+15] Y. A. Manerkar, D. Lustig, M. Pellauer, and M. Martonosi. "CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface". In: MICRO. 2015. DOI: 10.1145/ 2830772.2830782.